Module Title: Advanced Digital Design

Module Code: ENGD3001

**ADVANCED DIGITAL DESIGN**

**ASSIGNMENT 2**

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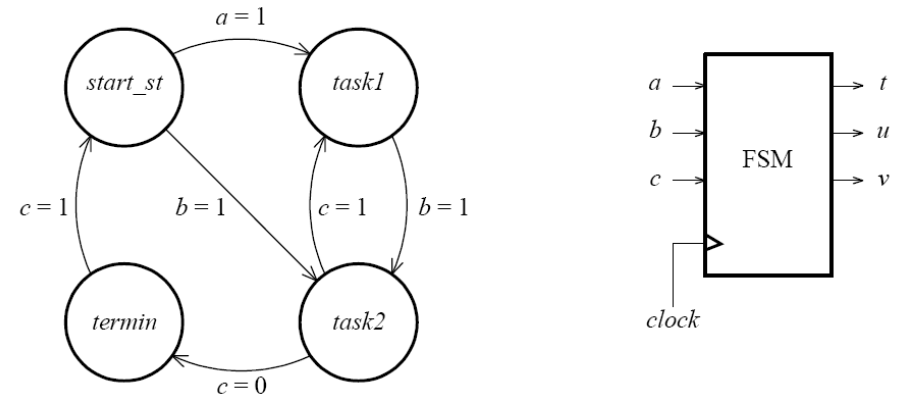
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# INTRODUCTION

This assigment focus the student to implement a VHDL code for a given finite state machine diagram. There are two basic types of state machines as Moore and Mealy. Both of the machines have timing clock. Vending macines, Elevator systerms, Goods carriage hoists, Traffic lights , are some example systems for behaviour of state Machines. Large programs can be implement by vhdl referencing FSM diagrams

1. Design Brief of Implementation of VHDL Code using FSM diagram

The Finite state machine should be analyse and should be implement a vhdl code then its behavioral should be analyse with the aid of a text-based testbench (A test bench written in VHDL)

Below figure illustrate the state transition diagram of a finite state machine that is going to implement the VHDL code

**Figure 1: State Transition Diagram**

As per the above figure three data inputs one parallel output are presented. They are,

Inputs: A

B

C

Output: T

U

V

As per the above diagram there are 4 different states clearly shows in the transition diagram. There are three digital inputs.The variations of the three digital inputs feedback the system to transition into relevent step (change the state).

A clock signal is synchronuosly supplying to the system. The Transitions happens along with the clock cycle synchronoulsy as according to the input signal

According to the states the t,u,v outputs are varying. Given below the table of outputs of the FSM as according to the state.

|  |  |  |  |
| --- | --- | --- | --- |
| **State** | **t** | **u** | **v** |
| *start\_st* | 0 | 0 | 0 |
| *task1* | 0 | 1 | 0 |
| *task2* | 1 | 1 | 0 |
| *termin* | 1 | 1 | 1 |

**Table 1: Outputs of the FSM**

The transition of state happen as a cycle and the clock input should be neccasary for the system to happen the transition.

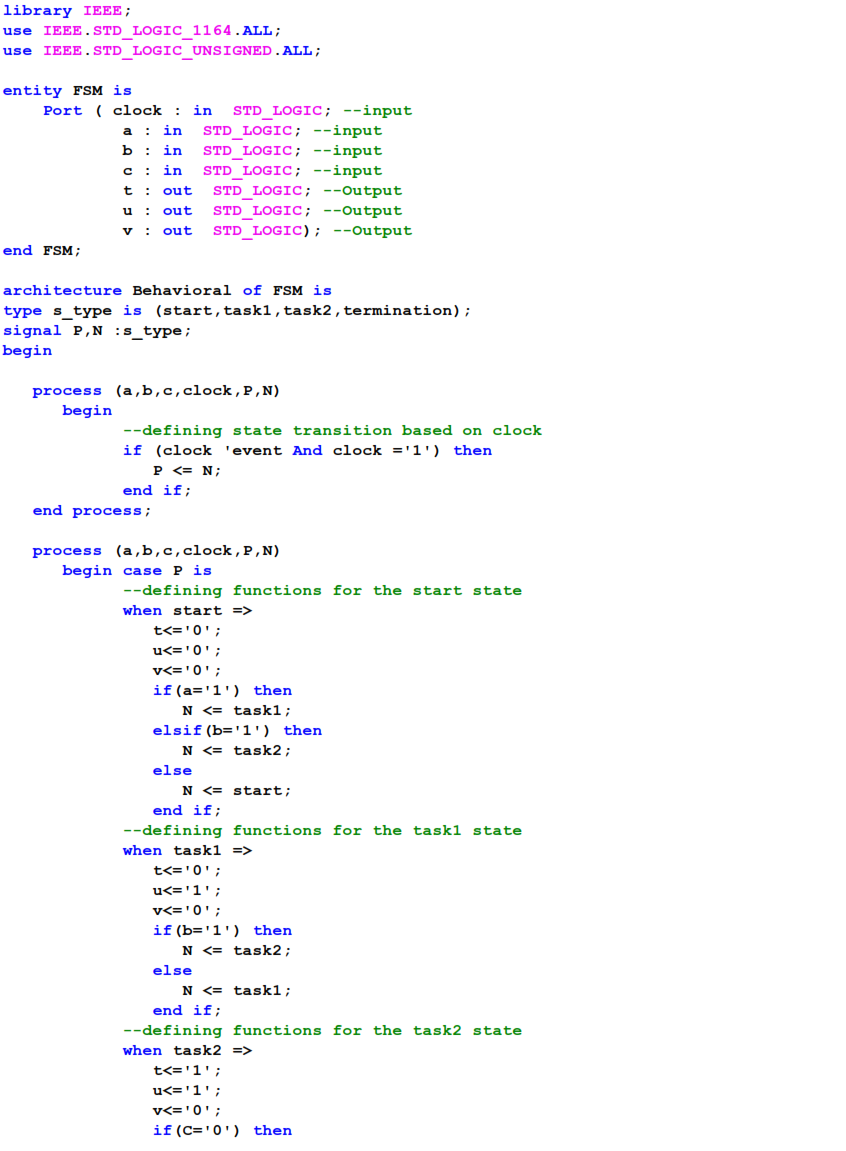
Very High-Speed Integrated Circuit Hardware Description Language also known as VHDL. Xilinx Vivado software is used in this assignment in order to program the design using VHDL and the Xilinx ISE design suite Software is used in order to simulate the behavioral model.

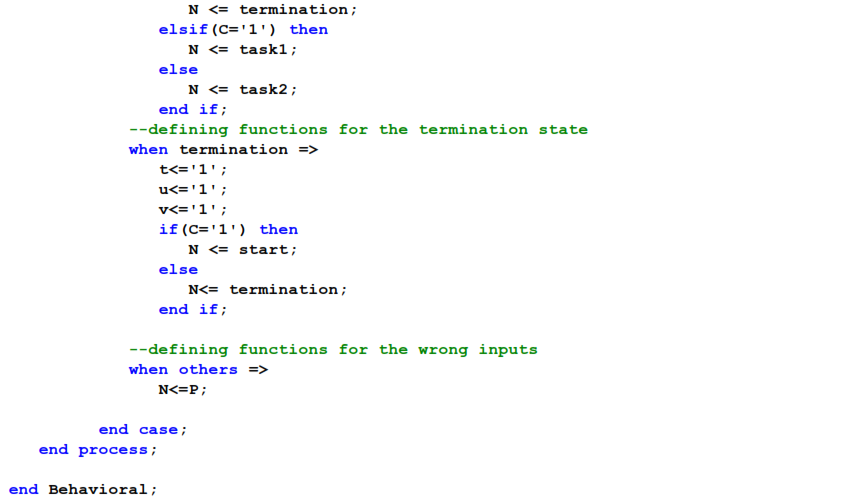
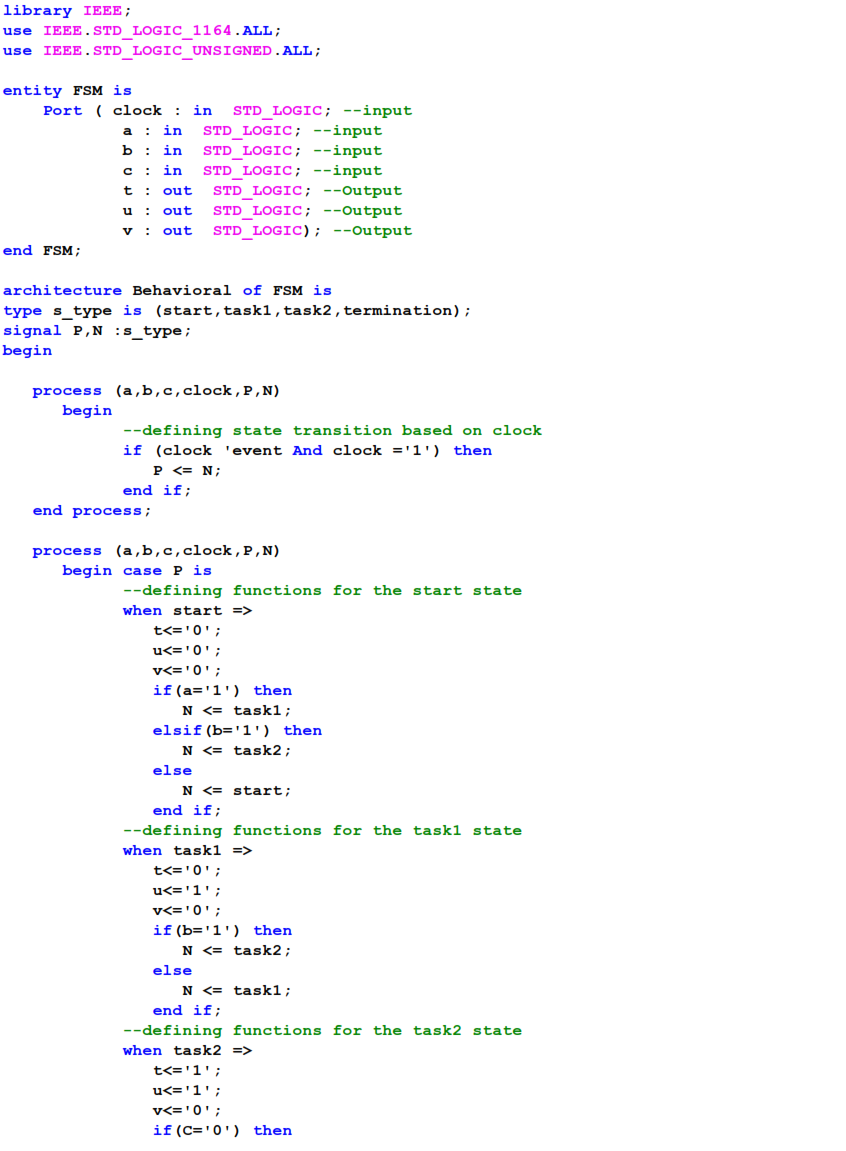
# BACKGROUND

## Pin Connections of the Design

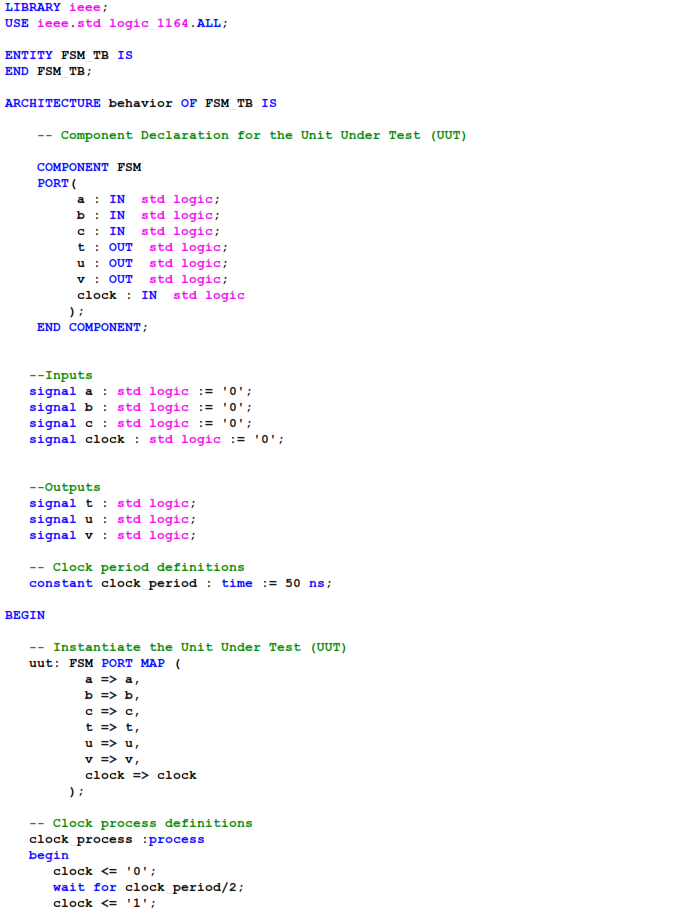
## Operation of the Designed

# VHDL CODES

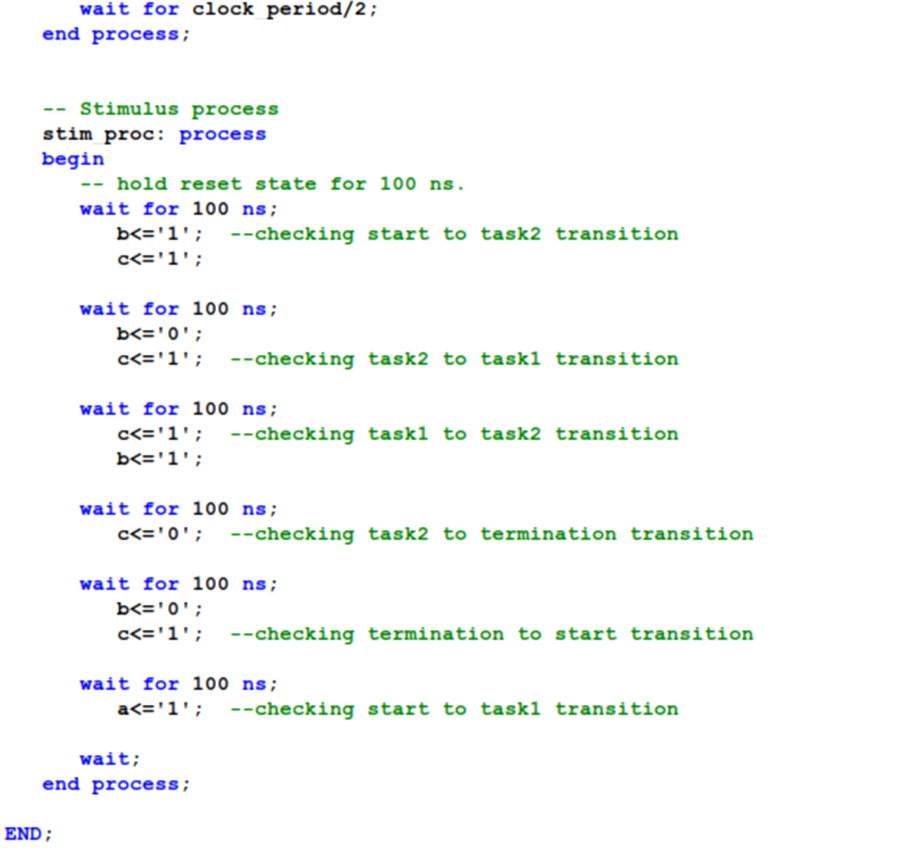
1. VHDL Code
2. Test Bench Coding
3. Vhdl Code



1. TestBench Code

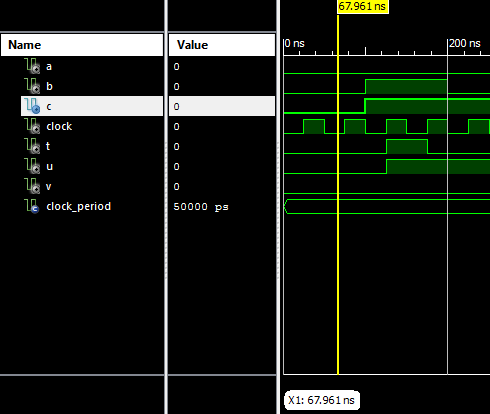






# SIMULATION WAVEFORMS

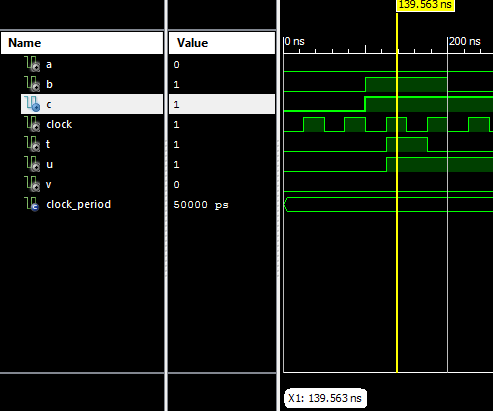
1. Start to task 2 transition



Comments-

Above figure illustrate the simulation at start state of the design. In here we can see the states are changed from start state to task 2 state when b becomes one (b=1) after the 100ns. As per the above figure and the simulation results we can confirm that the design is performing well at the start to task 2 change.

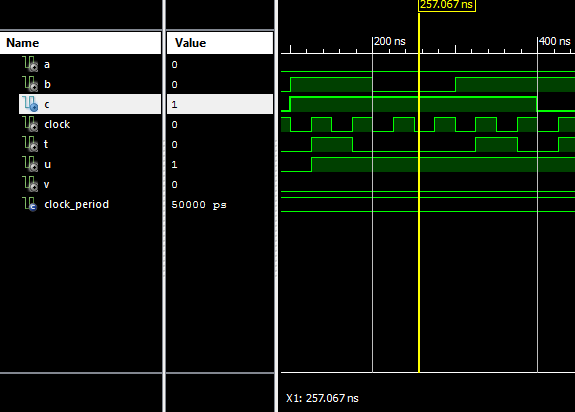
1. Task 2 to task 1 transition



Comments-

Above figure illustrate the simulation when the output at the task 2 state of the design. In here we can see the states are changed from task 2 to task 1 state because c is one (c=1) at the 175ns. As per the above figure and the simulation results we can confirm that the design is performing well at the task 2 to task 1 change.

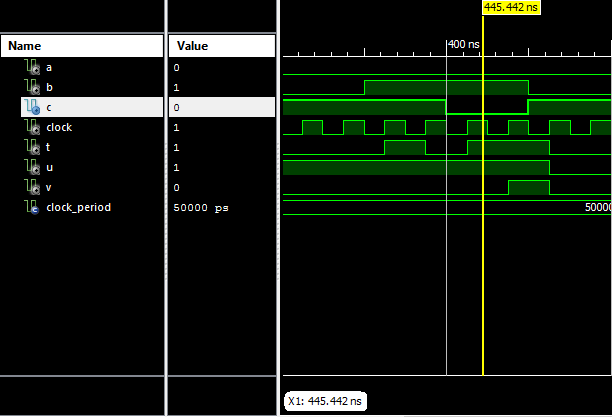
1. Task 1 to task 2 transition



Comments-

Above figure illustrate the simulation when the output at the task 1 state of the design. In here we can see that the states are changed from task 1 state to task 2 state because b becomes one (b=1) after the 325ns. As per the above figure and the simulation results we can confirm that the design is performing well at the task 1 to task 2 change.

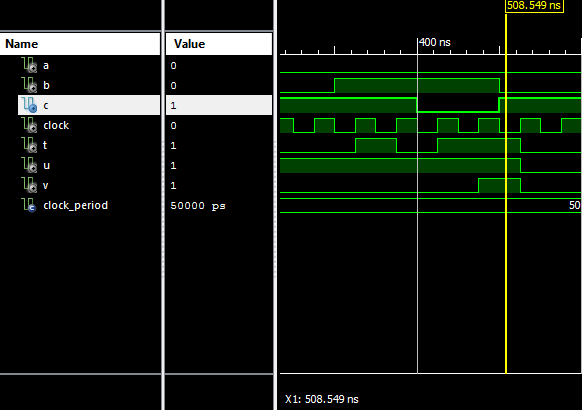
1. Task 2 to termination transition



Comments-

Above figure illustrate the simulation when the output at the task 2 state of the design. In here we can see that the states are changed from task 2 state to termination state because c is Zero (c=0) at the 475ns. Therefore, as per the above figure and the simulation results we can confirm that the design is performing well at the task 2 state to termination state change.

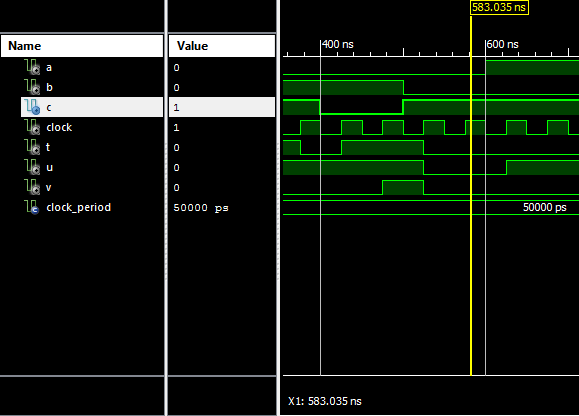
1. Termination to Start transition



Comments-

Above figure illustrate the simulation when the output at the termination state of the design. In here we can see that the states are changed from termination state to start state at the 525ns because c is 1 (c=1) at that point. Therefore, as per the above figure and the simulation results we can confirm that the design is performing well at the termination state to start state change.

1. Start to task 1 transition



Comments-

Above figure illustrate the simulation when the output at the start state of the design. In here we can see that the states are changed from start state to task 1 state at the 625ns because a is 1 (a=1) at that point. Therefore, as per the above figure and the simulation results we can confirm that the design is performing well at the start state to task 1 state change.

# CONCLUSION

Learned deeply into the approch of FSM designs, types of finite state machines like Melay and Moore machine

Learned deeply about how to do the VHDL coding for a given FSM. How to involve to do the design efficently with limited timeline.

Get a good understand about what is a clock pulse. How it is usefull when involving VHDL designs. Difference of synchrounus and asynchrounus clock

So far get a overall good knowladge about simulation of a VHDL code using a test bench code. We understood the simulation is a good practise to follow before finalising the code work in real world practical applications.

# REFERENCES

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